ABSTRACT

Emulation communications via a test access port and boundary-scan architecture providing serial access to a serial connection of a plurality of registers disposed in a plurality of modules. One of the modules is selected for communication. Nonselected moduled are made nonresponsive to data on the serial connection. The external emulation hardware supplys a serial signal having a first logic state for a number of cycles greater in number than a number of bits of the serial connection of registers to the test access port. The the emulation hardware supplys a start bit having an opposite logic state. The selected module detects the start bit and stores the next predetermined number of data bits. These bits could be data bits to be stored in a program visible data register or bits interpreted as an instruction for execution by the module. The selected module may transmit return communications via the serial scan path using the same format.